1 Overview

1.1 features

- IEEE 802.3-2008, IEEE 802.3az fully
- standards compliant
- IEEE 1588-2008 support
- Dual port MAC interface:

  GMII (10/100/1000BASE-T)

  MII (10/100BASE-T)
- Auto-negotiation support
- Automatic detection and correction of pair swaps (Auto-MDIX), pair skew and pair polarity
- 6 different operating modes:

  1000BASE-T Full Duplex and Half Duplex

  100BASE-TX Full Duplex and Half Duplex

  10BASE-T Full Duplex and Half Duplex
- Management interface
- Baseline wander compensation
- On-chip transmit wave-shaping
- On-chip hybrid circuit
- 10KB jumbo frames
- Internal, external and remote loop back
- Hardware configuration for default operation
- Power down mode, interrupt support
- LED indication: link mode, status, speed, activity, and collision
- Technology: 28nm 8ML

1.2 block diagrams

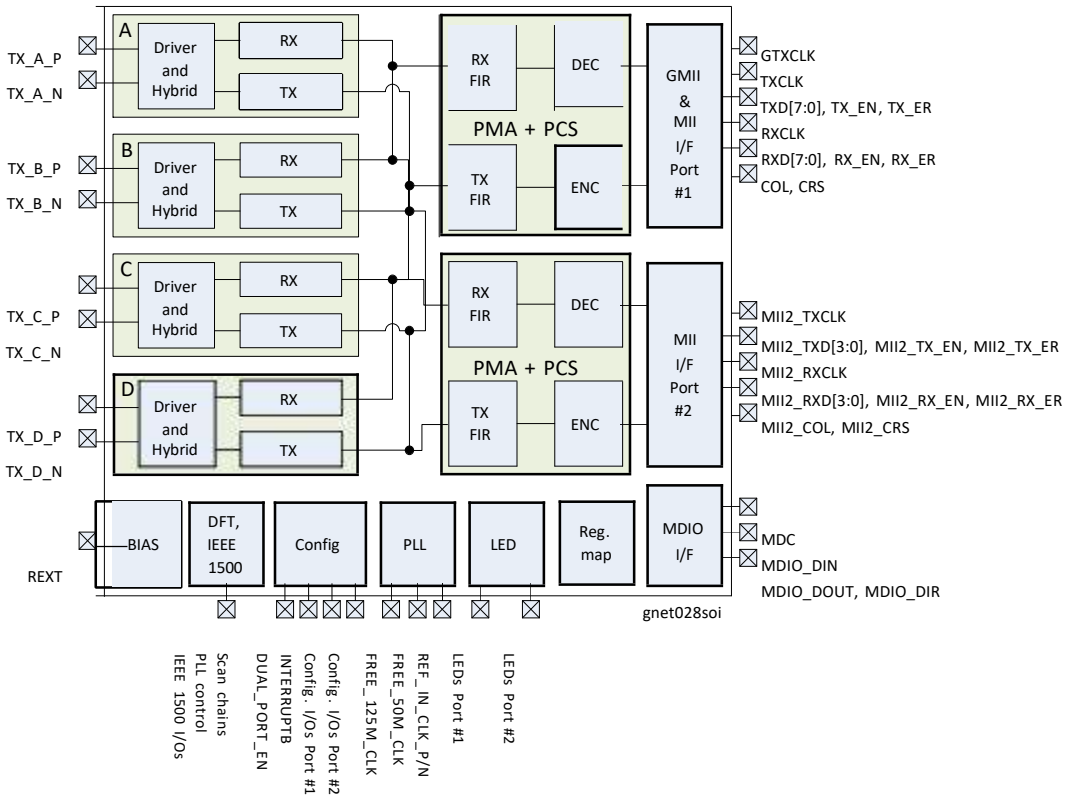


Figure1.1 block diagram

1.3 Functional block description

1.3.1 PLL

The PLL provides all the clocks required by the IP. It requires an external reference clock.

The VCO is based on a ring oscillator with multiple phase outputs.

The VCO lock frequency is 500 MHz when the IP is used in Ethernet legacy modes.

From this master clock two fixed dividers provides a 50 MHz and a 125 MHz clock source made available

1.3.2 Transmitter

The transmitter is following the 802.3 standard. Four instances are embedded into the IP to drive the four IP channels.

Each transmitter is based on a DAC coupled to a line driver trough filters to be compliant with harmonics requirements.

Driver is fully differential and the common mode is generated internally. The center tap of the line transformer does not require to be connected to any supply line, but must be decoupled with a capacitor to ground. See Appendix A for additional details on application external components.

The line termination is internal, and it is automatically calibrated to meet standard requirements. No external line termination resistors are required.

1.3.3 Receiver

The receiver is following the 802.3 standard. Four instances are embedded into the IP to get data from the four IP channels.

It is composed by VGA, analog domain filter, ADC and digital signal processing. The receiver includes also a signal detector used to manage EEE operations.

2 Pin description

The following sections describe the pins with related function.Pins are grouped by functions.

Power and Ground pins (VDD_DBE, GND_DBE) are not explicitly declared in the Verilog behavioral modules. They are described as pg_pin in the Liberty as well as verilog_all pins views.

2.1 Power supply pins

This pins group contains the power supply and ground pin used for the analog section.The digital section is powered by connecting its power grid to the digital power supply.Digital section power pins are VDD_DBE and GND_DBE.

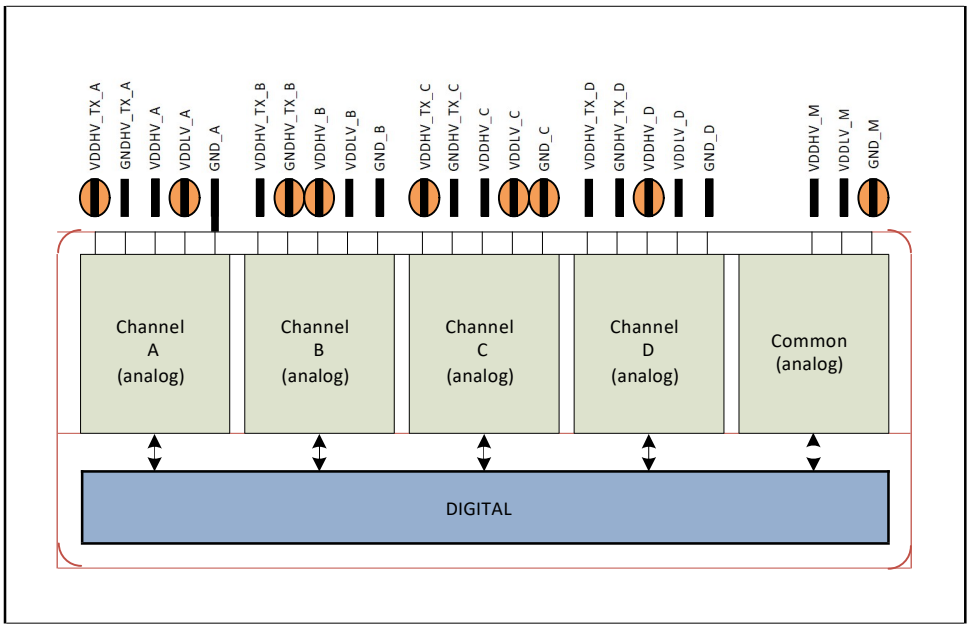


Figure2.1 Power supply pins

Table 2.1 Power supply pins list

IO name	Bus size	IO type	Description
GND_M	1	B	Common section Ground pin
GND_A	1	B	Channel section Ground pin
GND_B	1	B	Channel section Ground pin
GND_C	1	B	Channel section Ground pin
GND_D	1	B	Channel section Ground pin
GNDHV_TX_A	1	B	Channel section TX Driver High Voltage Ground pin
GNDHV_TX_B	1	B	Channel section TX Driver High Voltage Ground pin
GNDHV_TX_C	1	B	Channel section TX Driver High Voltage Ground pin
GNDHV_TX_D	1	B	Channel section TX Driver High Voltage Ground pin
VDDHV_M	1	B	Common section High Voltage Supply pin at 1.8V
VDDHV_A	1	B	Channel section High Voltage Supply pin at 1.8V
VDDHV_B	1	B	Channel section High Voltage Supply pin at 1.8V
VDDHV_C	1	B	Channel section High Voltage Supply pin at 1.8V
VDDHV_D	1	B	Channel section High Voltage Supply pin at 1.8V
VDDHV_TX_A	1	B	Channel section TX Driver High Voltage Supply pin at 3.3V

VDDHV_TX_B	1	B	Channel section TX Driver High Voltage Supply pin at 3.3V
VDDHV_TX_C	1	B	Channel section TX Driver High Voltage Supply pin at 3.3V
VDDHV_TX_D	1	B	Channel section TX Driver High Voltage Supply pin at 3.3V
VDDLV_M	1	B	Common section Low Voltage Supply pin at 0.9V
VDDLV_A	1	B	Channel section Low Voltage Supply pin at 0.9V
VDDLV_B	1	B	Channel section Low Voltage Supply pin at 0.9V
VDDLV_C	1	B	Channel section Low Voltage Supply pin at 0.9V
VDDLV_D	1	B	Channel section Low Voltage Supply pin at 0.9V

2.2 Twisted pairs interface pins

This pins group contains the eight pins used to connect, through the external isolation transformer, the four pairs of the network cable.

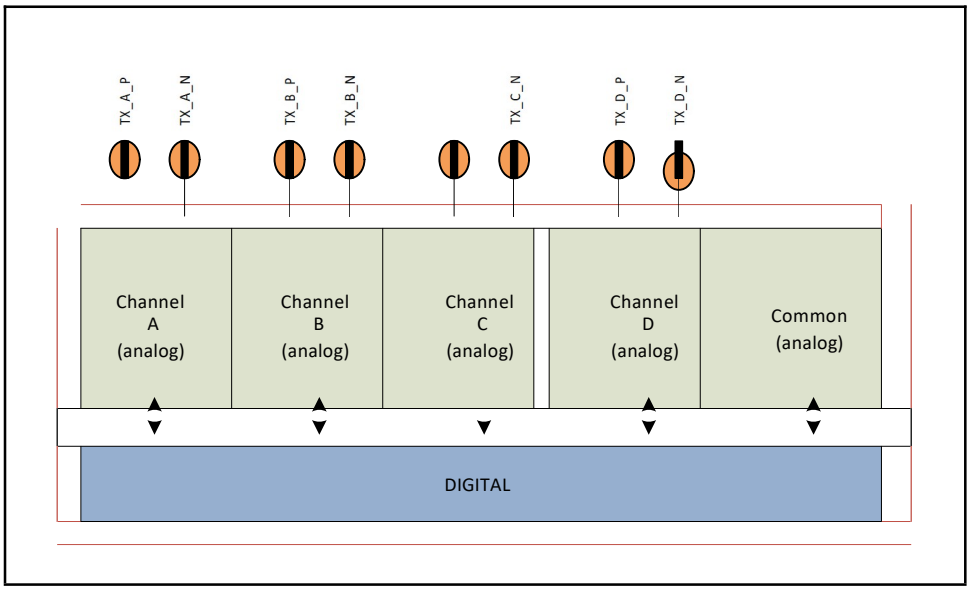


Figure2.2 Twisted pairs interface pins

Table 2.2 Twisted pair's interface pins list

IO name	Bus size	IO type	Description	Power domain
TX_A_N	1	B	Line A negative	VDDHV_TX_A, GNDHV_TX_A
TX_A_P	1	B	Line A positive	VDDHV_TX_A, GNDHV_TX_A
TX_B_N	1	B	Line B negative	VDDHV_TX_B, GNDHV_TX_B
TX_B_P	1	B	Line B positive	VDDHV_TX_B, GNDHV_TX_B
TX_C_N	1	B	Line C negative	VDDHV_TX_C, GNDHV_TX_C
TX_C_P	1	B	Line C positive	VDDHV_TX_C, GNDHV_TX_C
TX_D_N	1	B	Line D negative	VDDHV_TX_D, GNDHV_TX_D
TX_D_P	1	B	Line D positive	VDDHV_TX_D, GNDHV_TX_D

2.3 Analog test pins

This pins group contains the two pins used for testing and debugging of the analog sections.It is not recommended, as it is limiting the debugging activity.

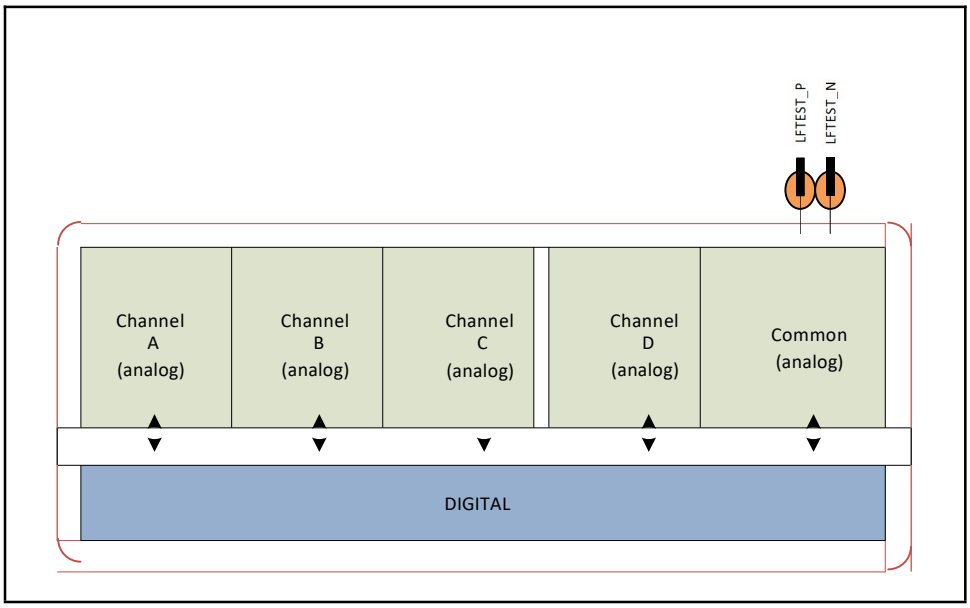


Figure2.3 Analog test pins list

Table 2.3 Analog test pins list

IO name	Bus size	IO type	Description	Power domain
LFTEST_N	1	O	Low frequency test negative	VDDHV_M, GND_M
LFTEST_P	1	O	Low frequency test positive	VDDHV_M, GND_M

2.4 Analog reference and clock

This pins group contains the pins used to provide bias and clock reference to the analog section.

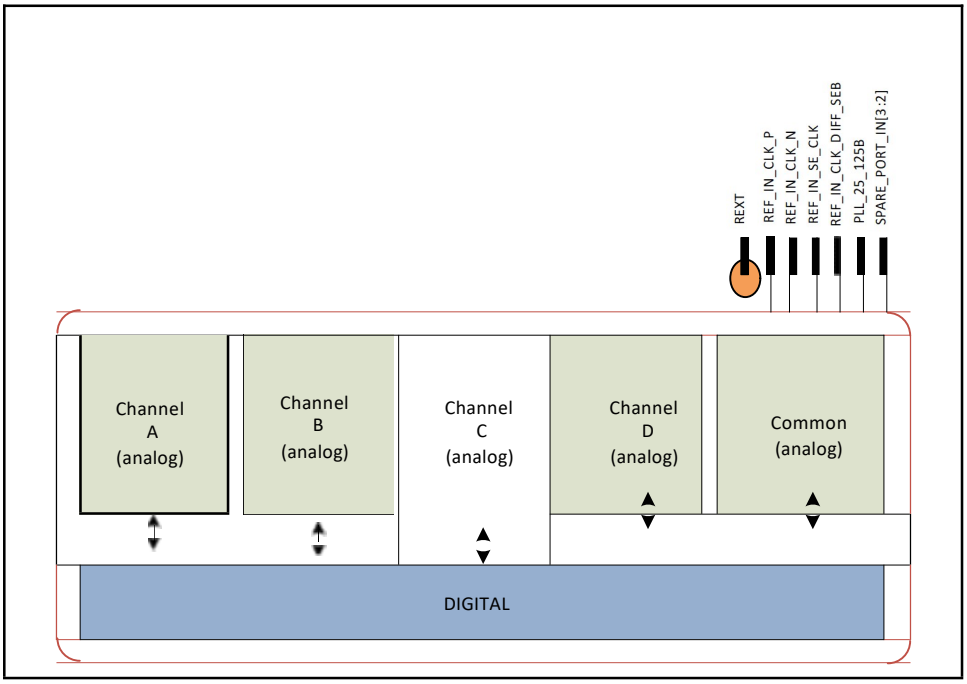


Figure2.4 Analog reference and clock pins

Table 2.4 Analog reference and clock pins list

IO name	Bus size	IO type	Description	Power domain
REXT	1	B	External reference resistor Value: 5 KOhm +/-1%.Note1	VDDHV_M, GND_M
REF_IN_CLK_P	1	I	Reference clock input positive (CML levels.Note2) This clock is expected to be active before releasing RESETB	VDD_M, GND_M
REF_IN_CLK_N	1	I	Reference clock input negative (CML levels) This clock is expected to be active before releasing RESETB	VDD_M, GND_M
REF_IN_SE_CLK	1	I	Single-ended reference clock input @ 0.9V This clock is expected to be active before releasing RESETB	VDD_DBE, GND
REF_IN_CLK_DIFF_SEB	1	I	Reference clock mode: 0: single-ended ref. Clock (use REF_IN_SE_CLK) 1: differential ref. clock (use REF_IN_CLK_P/N)	VDD_DBE, GND
PLL_25_125B, SPARE_PORT_IN[3:2]	3	I	Reference input clock frequency selection – seeTable 2.5.	VDD_DBE, GND

Note1： An external 4.99KOhm +/- 1% resistor is also in specification

Note2： REF_IN_CLK_P/N can be alternatively fed with signal working at CMOS levels.

Table 2.5 Reference clock selection

SPARE_PORT_IN[3]	SPARE_PORT_IN[2]	PLL_25_125B	Ref. clock freq.	Notes
0	0	0	125 MHz	Legacy
0	0	1	25 MHz	Legacy
0	1	X	30 MHz	
1	0	X	40 MHz	
1	1	X	Reserved	Mapped to 40 MHz

Note： For ESD (CDM) protection reason, it strongly recommended to drive the possible constant value through a buffer, avoiding direct tie high/low.

2.5 MDIO interface pins

This pins group contains the pins used by the MDIO interface.All pins are under the VDD_DBE, GND_DBE power domain.

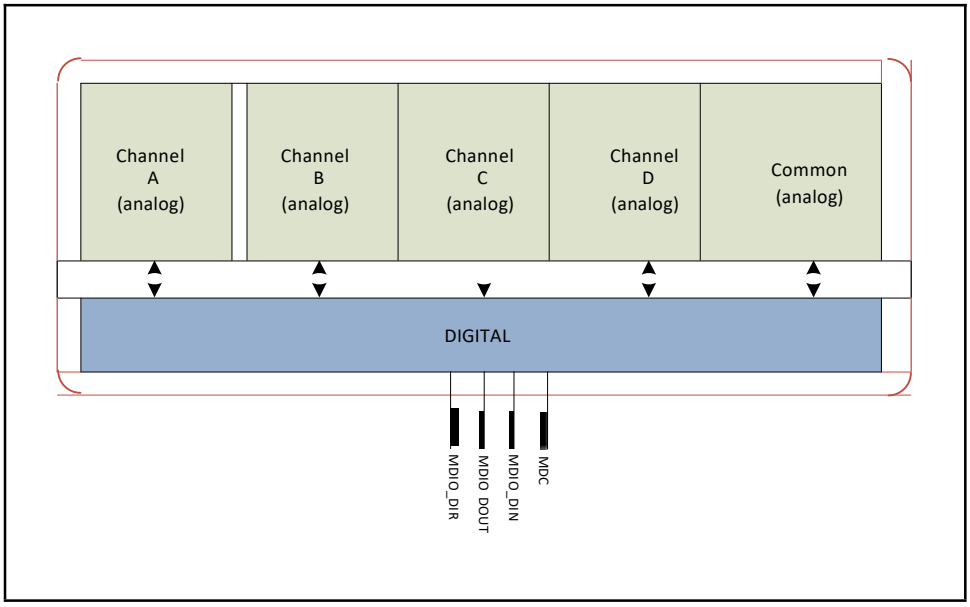


Figure 2.5 MDIO interface pins

Table 2.6 MDIO interface pins

IO name	Bus size	IO type	Related Pin	Description
MDC	1	I		MDIO clock Min period: 400 ns regardless TXCLK/GTXCLK/RXCLK
MDIO_DIN	1	I	MDC	MDIO input serial data
MDIO_DOUT	1	O	MDC	MDIO output serial data
MDIO_DIR	1	O	MDC	MDIO pad direction

2.6 GMII / MII interface

MAC interface is supporting 10/100/1000BASE-T mode in single port operation.This pins group contains the pins used by the GMII/MII interface.Figure 2.6 contain the description of the pins used by the GMII/MII interface .All pins are under the VDD_DBE, GND_DBE power domain.

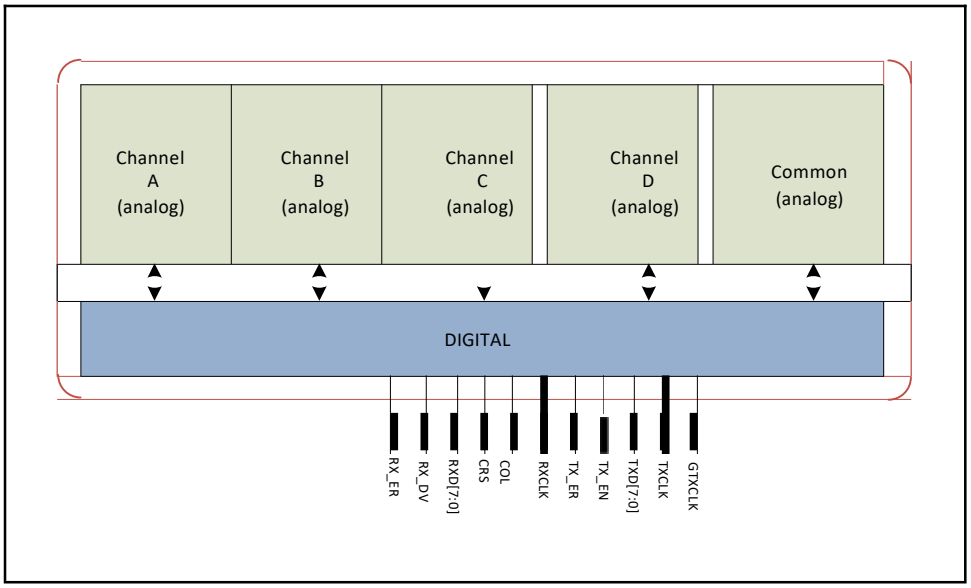


Figure2.6 GMII/MII pins for interface

Table 2.7 GMII/MII pin list for interface

IO name	Bus size	IO type	Related Pin	Description
GTXCLK	1	I		GMII TX clock Freq. 125 MHz Active in 1000 BASE-T mode
TXCLK	1	O		MII TX clock Freq. 25 MHz in 100 BASE-T. Freq. 2.5 MHz in 10 BASE-T.
TXD	8	I	GTXCLK TXCLK	TX data Bits 7:4 are used in 1000 BASE-T mode,only
TX_EN	1	I	GTXCLK TXCLK	TX enable
TX_ER	1	I	GTXCLK TXCLK	TX error
RXCLK	1	O		MII/GMII Rx clock Freq. 125 MHz in 1000 BASE-T. Freq. 25 MHz in 100 BASE-T. Freq. 2.5 MHz in 10 BASE-T.
COL	1	O		Collision detect
CRS	1	O		Carrier Sense
RXD	8	O	RXCLK	Rx data Bits 7:4 are used in 1000 BASE-T mode, only
RX_DV	1	O	RXCLK	Rx data valid
RX_ER	1	O	RXCLK	Rx error

2.7 Configuration pins

This pins group contains the pins used for the direct configuration of the IP modes.Figure 2.7 contains all configuration pins.Table 2.8 contains the PHY mode configuration pin description,Table 2.9 contains the configuration pin.

All these signals have to be set and stable before releasing RESETB. Any change on these signals while RESETB=1 will not have effect as long as the user toggles RESETB.

Changing the value DUAL_PORT_EN when the PHY is active, i.e. RESETB=1 may cause unpredictable behavior, so the user is recommended to keep it stable while operating.

All pins are under the VDD_DBE, GND_DBE power domain.

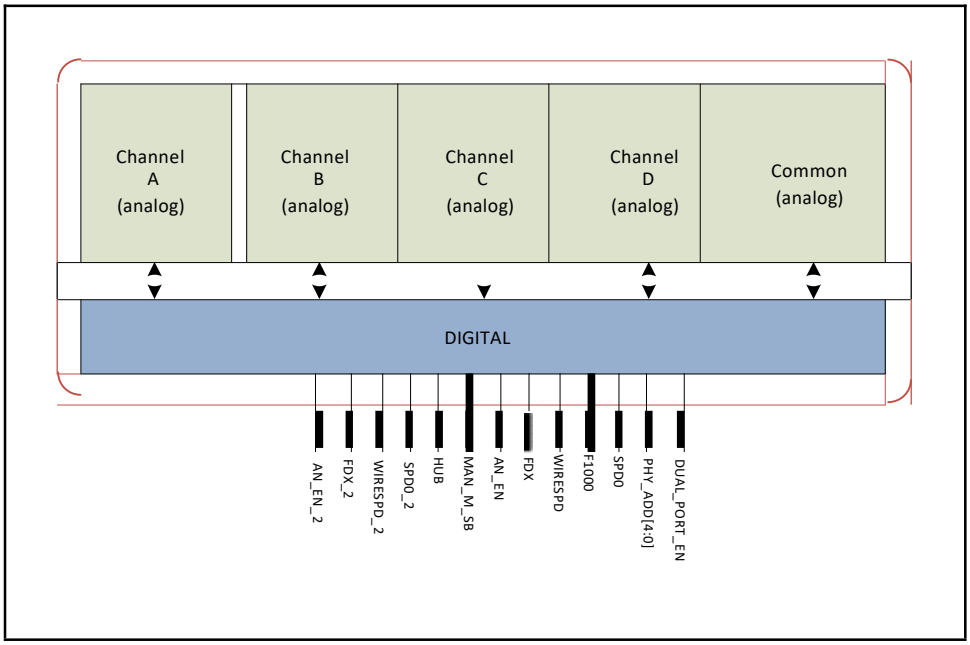


Figure2.7 Configuration pins

Table 2.8 PHY mode configuration pins

IO name	Bus size	IO type	Description	Connection at SoC Pad type
PHY_ADD	5	I	PHY address. The values on these pins are latched at reset.	Set to anything different from 00000. 00000 is reserved (broadcast).

Table 2.9 Configuration pins

IO name	Bus size	IO type	Description	Connection at SoC Pad type
SPD0	1	I	Speed selection {F1000, SPD0} 00: 10 BASE-T 01: 100 BASE-T 10: 1000 BASE-T 11: Reserved	Not considered when AN_EN=1.
F1000	1	I		
WIRESPD	1	I	Wire Speed Downgrade Active high	Not considered when AN_EN=1.
FDX	1	I	Full duplex enable Active high	

AN_EN	1	I	Auto-negotiation enable Active high	
MAN_M_SB	1	I	Manual master/slave enable 0:Disable M/S manual configuration (M/S resolved by Auto-negotiation) 1: Enable M/S manual configuration	Not considered in 10/100Base-T mode
HUB	1	I	Manual master/slave value Applicable only when MASTER/SLAVE manual configuration is enabled 1 = Configure IBST8820 as a Master PHY 0 = Configure IBST8820 as a Slave PHY	Not considered in 10/100Base-T mode

2.8 Miscellaneous control and debug pins

This pins group contains the pins used for testing, the clocks outputs and the reset control pins.All pins are under the VDD_DBE, GND_DBE power domain.

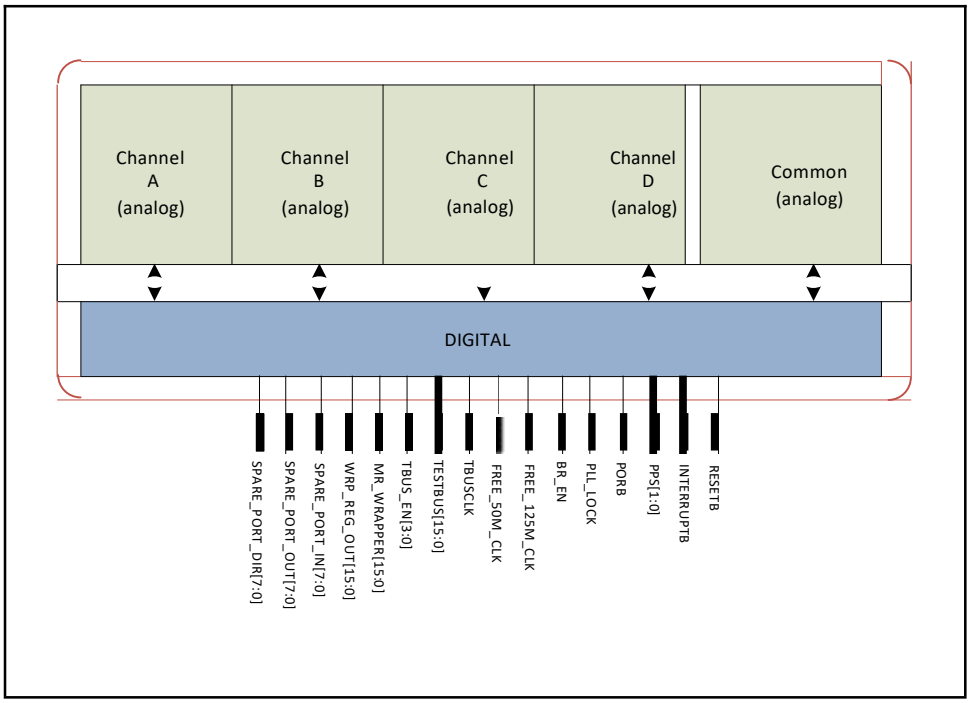


Figure2.8 Miscellaneous control and debug pins

Table 2.10 Miscellaneous controls and debug pins list

IO name	Bus size	IO type	Related Pin	Description
RESETB	1	I	RESETB	Main reset. Active low Asynchronous (internally re-synchronized)
INTERRUPTB	1	O	INTERRUPTB	Interrupt line. Active low The events generating an interrupt can be selected through a user register – see below.
PPS	2	O		Pulse Per Second
PORB	1	O		Power-on reset. Active low Power-on reset. Active low Semi static signal that indicates the 0.9V supply (VDDLV_M) has reached a minimum threshold. It can be observed with a register.
PLL_LOCK	1	O		PLL lock, active high
BR_EN	1	I		BroadR-Reach™ enable. When set to '1' BRR IP

				is configured in such mode. Enable is internally disabled when IP is not explicitly requiring it
FREE_125M_CLK	1	O		Free running 125 MHz clock (137.5 MHz when BroadR-Reach™ mode is enabled) It is driven to 0 when RESETB=0. It will start toggling at the nominal frequency after power up time, i.e. ~100us after releasing RESETB.
FREE_50M_CLK	1	O		Free running 50 MHz clock (55 MHz when BroadR-Reach™ mode is enabled) It is driven to 0 when RESETB=0 or mr_soc_pll_free_50m_clk_en register[Note1] is set to 0. It will start toggling at the nominal frequency after power up time, i.e. ~100us after releasing RESETB.
TBUSCLK	1	O		Digital test bus clock
TESTBUS	16	O	TBUSCLK	Digital test bus
TBUS_EN	4	O	TBUSCLK	Digital test bus: trigger signal output
MR_WRAPPER	16	O		Register o/p for test chip wrapper configuration
WRP_REG_OUT	16	I		Register i/p for test chip wrapper configuration
SPARE_PORT_IN	18	I		Spare ports input 17:10: unused 9: 1500 regmap intercept. See [3] 8: OCC dedicated reset in test mode (it resets the OCCs when DFT_MODE is 1) 7: boundary scan enable 6:5: boundary scan channel selection 4: boundary scan data 3:2: see Reference clock selection 1: unused 0: trigger input for IEEE 1588
SPARE_PORT_OUT	18	O		Spare ports output 17:4: unused 3: zero 2: IEEE 1588 trigger out 1:0: zero
SPARE_PORT_DIR	18	O		Spare ports direction

Note1： Bit 0 of register 20 in page 30, disabled when DFT_MODE is set to

2.8.1 Interrupt description

The interrupt feature is enabled by the custom register 0x10, bit 0. The value 0 means the interrupt is active. Default value is 0.

Each interrupt event can be masked using the custom register at page 9 (write 9 on reg 0x010[13:8]), register 0.x17. Setting the corresponding bit to 1 means the event is active.

The interrupt status register is at page 9 (write 9 on reg 0x010[13:8]), reg 0x018.

A user interrupt can be generated generating a positive transition (0 ->1) on the bit 6 at page 9 (write 9 on reg 0x010[13:8]), register 0x16.

The complete list of interrupt events available is below.

Table 2.11 Interrupt event list

Mask bit	Description
15	Manual/user interrupt
14	IEEE1588 Triggered out
13	IEEE1588 PPS
12	IEEE1588 new IN Timestamp
11	IEEE1588 new TX Timestamp
10	IEEE1588 new RX Timestamp
9	CRC32 error detected
8	LPI detected
7	False carrier detected
6	Descrambler sync lost
5	Jabber detected
4	Auto crossover change
3	AN fault
2	AN new page received
1	AN complete
0	Link status change

2.9 LED interface

This pins group contains the pins used for the LED status.All pins are under the VDD_DBE, GND_DBE power domain .

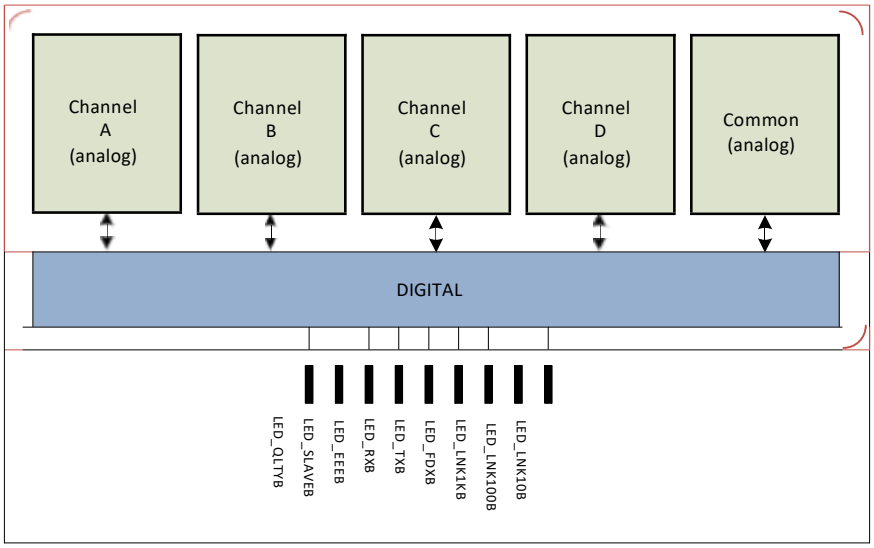


Figure2.9 LED interface pins

Table 2.12 LED interface pins

IO name	Bus size	IO type	Related Pin	Description
LED_LNK10B	1	O		PHY is operating in 10B-T mode. Active low
LED_LNK100B	1	O		PHY is operating in 100B-T mode. Active low
LED_LNK1KB	1	O		PHY is operating in 1000B-T mode. Active low
LED_FDXB	1	O		PHY is operating in Full-duplex mode. Active low
LED_TXB	1	O		Active for approximately 80ms each time a packet is transmitted. Active low
LED_RXB	1	O		Active for approximately 80ms each time a packet is received. Active low
LED_EEEB	1	O		EEE capability after auto-negotiation. Active low
LED_SLAVEB	1	O		PHY is operating in slave mode. Active low
LED_QLTYB	1	O		LED for poor link quality. Active low

The status of the LED's can be manually forced by the user using the following custom registers:

mr_ledoff: it forces the LEDs off. Register 0x11, bit 9.

mr_ledon: it forces the LEDs on. Register 0x11, bit 10.

Table 2.13 LED forcing description

mr_ledon	mr_ledoff	LED status
0	0	Normal mode (default). LEDs' status depends on PHY activity
0	1	LEDs forced off
1	0	LEDs forced on
1	1	LEDs forced off

3 Configuration & power modes

3.1 Power modes

Table 3.1 Power modes

Mode	Activated by	Status
Reset mode	RESETB = 0	PLL is off TX is off RX is off Register map and MDIO are reset
PLL-only mode	RESETB = 0 DFT_MODE = 1 Sequence described in Chapter3.1.1	PLL is on TX is off RX is off Register map and MDIO are reset
Normal mode	RESETB = 1	PLL is on TX is on RX is on Register map and MDIO are active

3.1.1 PLL only mode activation

The following timing drawing specifies the sequence needed to activate the clock generation for the SoC.

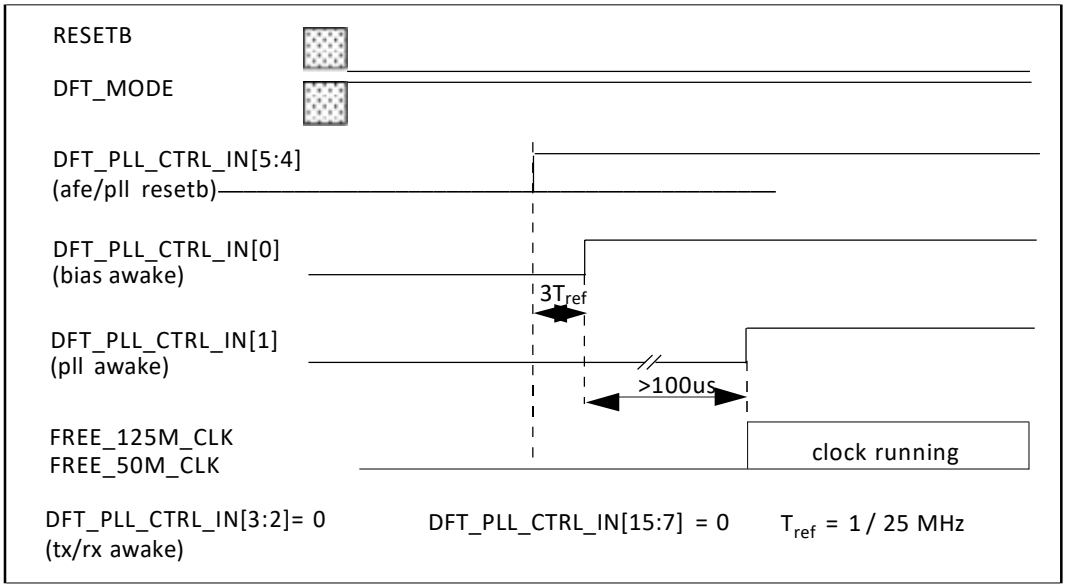


Figure3.1 PLL-only mode activation sequence

3.1.2 Power up times

The following table list the time needed for power up.

Table 3.2 Power up time

Mode	Time to be ready (min)
Reset mode	200 ns
PLL-only mode	110 us
Normal mode	110 us

3.1.3 Clock definition for power and reset states

Table 3.3 Clocks definitions for each power mode

Power mode	FREE_125M_CLK FREE_50M_CLK	TXCLK RXCLK
Reset mode	Off	Off
PLL-only mode	On	Off
Normal mode	On	On

3.2 10BASE-Te

The 10Base-Te mode, i.e. 10Base-T energy saving mode, can be activated through the following sequence of management registers.

Table 3.4 10BASE-Te selection

Custom configuration register	Shadow page	Register
mr_tx10_te_a_en=1	write 'd15 reg0x10[13:8]	write 'd1 reg0x15[4]
mr_tx10_te_b_en=1	write 'd15 reg0x10[13:8]	write 'd1 reg0x15[5]

4 Clocks and resets

4.1 Overview

The macro provides two free-running clocks, FREE_125M_CLK and FREE_50M_CLK, two functional clocks, TXCLK and RXCLK and two additional functional clocks, MII2_TXCLK and MII2_RXCLK, in case of dual port operation.

The macro needs to receive few external clocks to operate:

- Refclock for the internal PLL on pins REF_IN_CLK_P/REF_IN_CLK_N. Input may be configured as single ended or differential. This clock is considered to be free-running and always stable and active when the macro is active,i.e. either in PLL-only or normal mode. If this clock is not provided, all the output clocks, FREE_50M_CLK, FREE_125M_CLK, RXCLK, TXCLK,MII2_TXCLK, MII2_RXCLK are not generated, i.e. no toggling.
- Clock for the GMII TX interface on pin GTXCLK.
- Clock for the MDIO interface on pin MDC. It may be continuous. It is also specified by IEEE 802.3 clause 22.2.2.11.Interface clock diagram.

4.2 Clock signals

4.2.1 Free-running clocks

- FREE_125M_CLK: frequency 125 MHz (137.5 MHz in BroadR-Reach mode)
- FREE_50M_CLK: frequency 50 MHz (55 MHz in BroadR-Reach mode)

The free-running clocks are available after the internal PLL has locked – seeFigure4.1

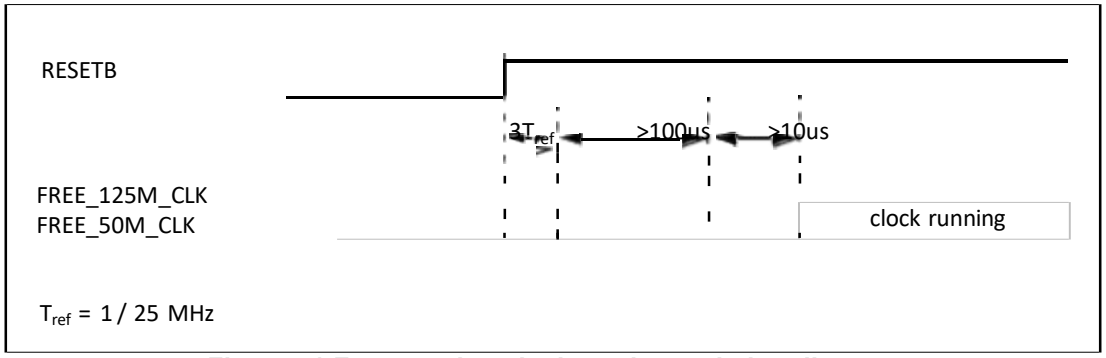


Figure4.1 Free running clocks wake up timing diagram

4.2.2 TX clocks

Depending on the selected transmitting speed (10Mb/s, 100Mb/s, 1Gb/s), either one of the following clocks are used to clock in data into the MII/GMII i/f:

TXCLK/MII2_TXCLK: it is active when 10 BASE-T or 100 BASE-T selected, i.e. MII is used. It is specified by IEEE 802.3 clause 22.2.2.1.

- 10 BASE-T: frequency: 2.5 MHz
- 100 BASE-T: frequency: 25 MHz

GTXCLK: it has to be active once the 1000BASE-T link has been acquired, i.e. GMII is used; its frequency is 125 MHz. This clock is also specified by IEEE 802.3, clause 35.4.2.3.

4.2.3 RX clocks

RXCLK/MII2_RXCLK: it is active when either MII or GMII interface is selected. It is also specified by IEEE 802.3 clause 22.2.2.2 and clause 35.2.2.2.

- 10 BASE-T: frequency 2.5 MHz
- 100 BASE-T: frequency 25 MHz
- 1000 BASE-T: frequency 125 MHz

4.3 Reset signals

There are two ways to apply resets to the macro see Table 4.1:

- Using the reset pins of the macro, RESETB
- Using soft resets through the management register(s), via MDIO interface

In all cases, these resets are asynchronous. The reset removal is synchronized internally on each clock domain for a correct start-up.See Section3.1.3 Clock definition for power and reset states for additional details.

Table4.1 Reset description

Port name/Register	Description	PHY core	Management regs	PLL
RESETB	Main reset. Active low. When it is active, the analog and digital circuits are reset, including the register map.	Yes	Yes	Yes
RN00[15]	Soft reset. Active High. Auto de-assertion.	Yes	Yes	No
RN00[11]	Digital reset. Active High. It resets the digital circuit.	Yes	No	No

Note：In this table, “Yes”and “No” means that the related sub-systems are under reset when the corresponding command is active; e.g. when the user writes 1 on reg.0.11 (=power down reset active), the PHY core will be reset, while the management registers as well as the PLL will not.For ATPG/test mode, RESETB is the primary input controlling the reset pins of all the scanned flip-flops of the macro cell.

4.3.1 Reset timing constraints

In normal mode of operation, the RESETB must guarantee the timing relationship with respect to MDC depicted in Figure 4.2 . This constraint is to allow a proper initialization of the macro from the external pins (seeTable 2.8 and Table2.9).

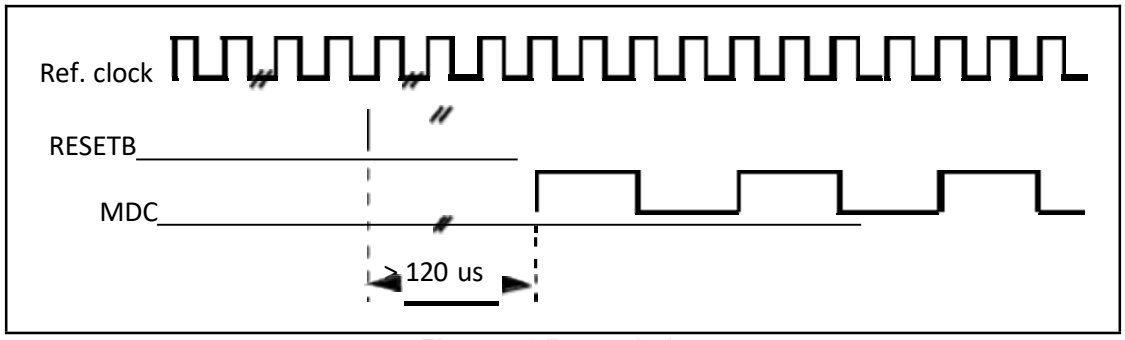


Figure4.2 Reset timing

4.3.2 Reset/clock relationship

1.RESETB is not required to be synchronous with any available clock;

2.Free running clocks, FREE_50M_CLK/FREE_125M_CLK, may glitch upon RESETB assertion;

3.All the available clocks are glitch-free after RESETB release

5 MDIO - Register interface

5.1 MDIO reference on IEEE 802.3

The management register access is specified on IEEE 802.3, clauses 22.2.2.11, 22.2.2.12, 22.2.4.5, 22.3.4. The following paragraphs reports a summary for the functional description as well as timing requirements.

5.2 MDIO Functional description (ref. IEEE 802.3, clause 22.2.4.5)

MDIO is a synchronous serial interface made up of two lines: MDIO (bi-directional data line, MDC clock). The data are launched/captured on the rising edge of the clock.

Each MDIO operation, write or read, is made up of seven fields: preamble, start of frame (ST), operation id (OP), PHY address (PHYAD), register address (REGAD), turn-around bits (TA), register data.

The Figure5.1 and Figure5.2 show a timing description of the two operations; note that MDIO dir is not part of the interface, but it has been shown as auxiliary information.

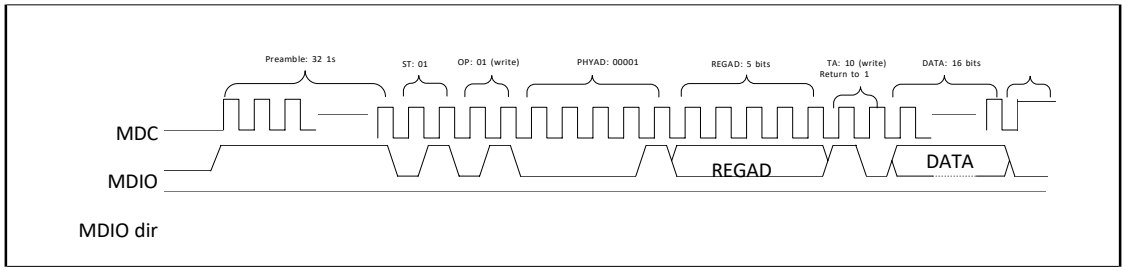


Figure5.1 MDIO write operation

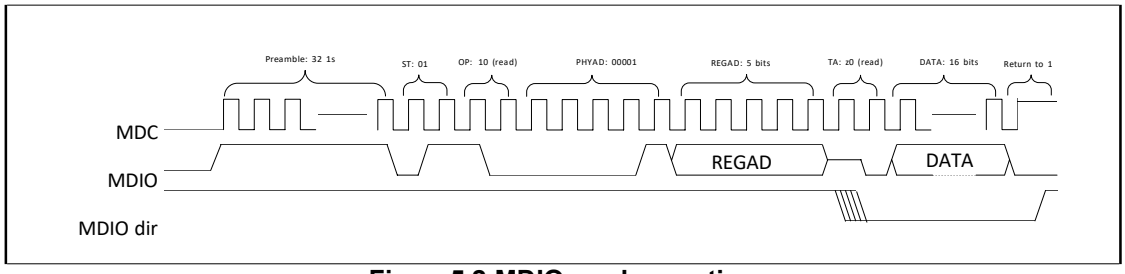


Figure5.2 MDIO read operation

The field PHYAD is a provided through the PHY_ADD – seeTable2.8

Each register is addressed by a 5-bit address (REGAD), while its content is 16-bit wide (DATA). The fields REGAD and DATA are separated by two turn-around bits.

6 Electrical specifications

6.1 Absolute maximum ratings and operating ranges

Table 6.1 Maximum ratings

Parameter	Min	Typ	Max	Unit
Analog supply VDDHV_TX at IO pins	3.0	3.3	3.6	V
Analog supply VDDHV at IO pins	1.65	1.8	1.95	V
Analog supply VDDLV and digital supply VDD_DBE at IO pins	0.9	1.0	1.1	V
Digital input voltage	VDD_DBE-0.3		VDD_DBE+0.3	V
Electrostatic discharge				
Human body model (HBM) EIA/JESD22-A114F	2000			V
Machine model (MM) EIA/JESD22-A115B	100			V
Charge device model (CDM) EIA/JESD22-C101E	500			V
Ambient temperature	0		70	℃
Tj Junction Temperature	-40	25	125	℃

6.2 Reference clock specifications

IBST8820 IP requires one reference clock input that must be provided to the IP on the pins REF_IN_CLK_P, REF_IN_CLK_N.

Voltage domain of this input is the low voltage (1.0V typ) analog domain.

Signal is single ended full swing; electrical characteristics are shown in the following table.

SeeTable2.5 for further details on REFCLOCK possible frequencies.

Table 6.2 Reference clock input specifications

Parameter	Min	Typ	Max	Unit
Duty Cycle	40	50	60	%
Rise/Fall time (20% to 80%)			200	ps
Phase jitter (RMS, low pass filtered @ 20 MHz)			40	ps
Precision			+/-50	ppm

REF_IN_CLK_P and REF_IN_CLK_N can also be provided as CML signals, in this case following constraints must be followed:

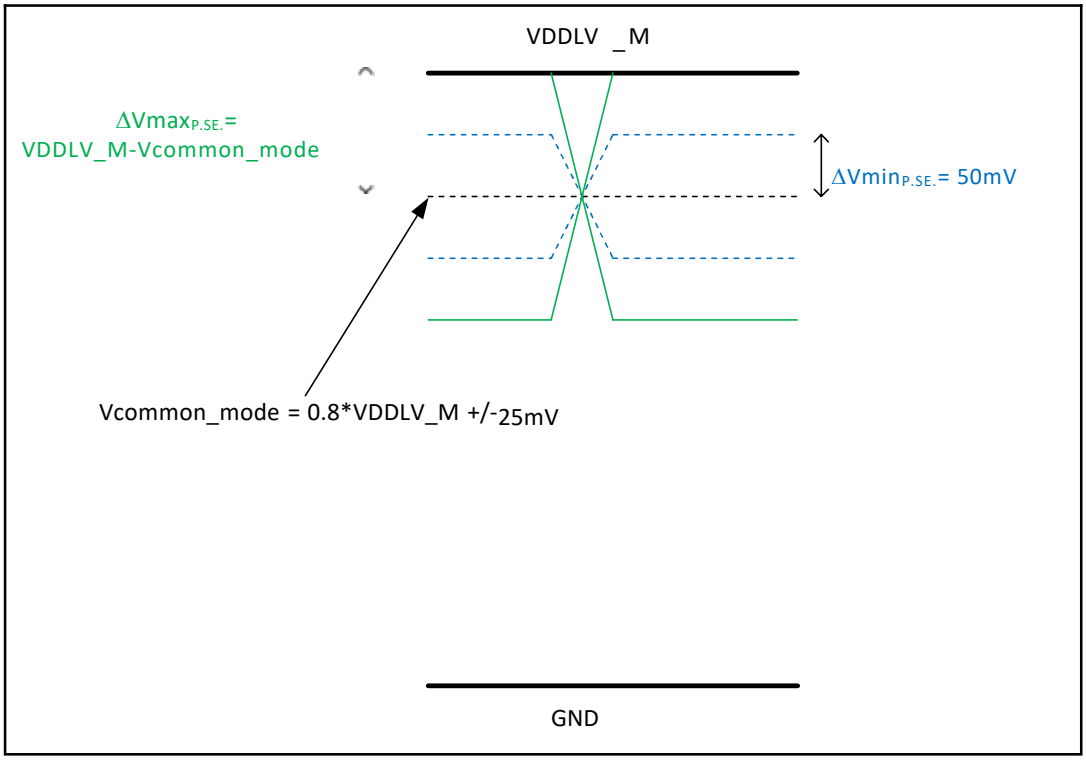


Figure6.1 REF_IN_CLK CML levels constraints

6.3 Power consumption

Next tables show the total power consumption of IBST8820 in different conditions.

Two different temperatures are shown in the tables .

Power figures in 10/100BT are considering both ports activated.

Values are shown for typical condition, that means typical process and nominal voltage supply, and worst case, that means fast process and maximum voltage supply as forTable6.1.

Table 6.3 IBST8820 power consumption typical condition

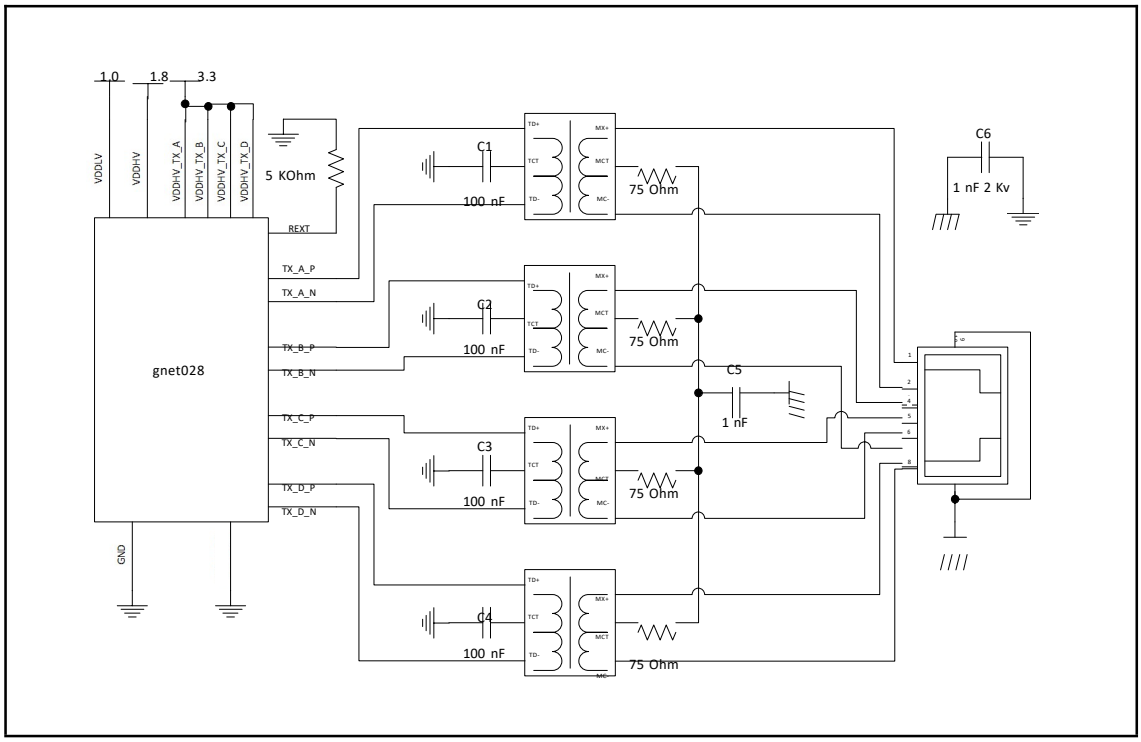
Mode	Total power @ 80°C [mW]	Total power @ 125°C [mW]
PLL only	9	10
Auto negotiation	272	270
10BASE-T	272	270
10BASE-Te	264	258
100BASE-TX	193	190
100BASE-TX QUIET MODE (EEE)	72	67
1000BASE-T	461	431
1000BASE-T QUIET MODE (EEE)	120	114

Table 6.4 IBST8820 power consumption worst case

Mode	Total power @ 80°C [mW]	Total power @ 125°C [mW]
PLL only	10	11
Auto negotiation	316	307
10BASE-T	316	307
10BASE-Te	305	283
100BASE-TX	212	207
100BASE-TX QUIET MODE (EEE)	88	84
1000BASE-T	505	505
1000BASE-T QUIET MODE (EEE)	132	146

Appendix A: Application requirements

The IBST8820 requires a minimum set of external components to operate.The suggested application schematics for the full capable 10/100/1000 configuration is shown in Figure A.1.



FigureA.1 10/100/1000 GNETPHY suggested application schematic

A.1 External components

The few external components required must satisfy the electrical characteristics described in the following paragraphs.

A.2 Line transformer

The line transformer must satisfy the 802.3 standards in term on isolation and frequency behavior.

The transformer ratio required by IBST8820 is 1:1.

The center tap of the transformer side connected to IBST8820 pins should be connected to ground trough a decoupling capacitor of 100 nF.

The center tap of the transformer side connected to UTP cable should be connected to a network composed by a series resistor of 75 Ohm, one for each UTP pair, connected from the transformer center tap to a common node. The common node must be connected to the UTP socket ground shield trough one or more decoupling capacitors of 1 nF each.

The RJ45 connector ground shield, as for the standard requirements, must not be connected to PCB signal ground, but decoupled trough a couple of 1 nF capacitor with voltage capability at least of 2000 V.

To ensure a 100-ohm differential-impedance track, it is recommended to route signals on an external layer with a full or partial ground plane layer as the next internal adjacent layer. If the ground plane is partial, it must cover and exceed area below the TX and RX signal routing.

- Signal pair lengths: Exactly equal signal-pair lengths (to avoid skew) from the ball to the connector:
  - TX_n_P length = TX_n_N length
- Differential impedance: A 100 Ohm differential impedance must be ensured along the entire track length between the package pin and the connectors.
- Routing: Signal pairs should be routed in parallel with equal signal track inter-space distance on each pair along the entire track length (to ensure the 100-ohm differential impedance).
  - Reduce as much as possible and balance PCB vias in the differential traces
  - Avoid unrelated PCB vias in close proximity to differential traces
  - All tracks should be as direct and straight (short) as possible

A.2.1 Reset timing constraints

Provision must be made for an external reference resistor connection to the REXT pin:

The value required is 5 KOhm (+/- 1%). PCB trace of resistor connection must be done as short as possible avoiding possible cross-talk with noisy signals.

Ground connection of resistor should be done as close as possible to C28_IBST8820 analog signal ground.

A.3 Power-supply filtering

The IBST8820 requirements, in term of power supply filtering, depends on the board noise.

Generally speaking, IBST8820 is more sensitive to noise in the band of the Ethernet standard signal: 10-20 MHz when in 10BASE-T mode, 65- 125 MHz when in 100BAE-T or 1000BASE-T mode.

The most effective noise decoupling at this frequencies is composed by a small series resistance, taking into account IR drop associated, and small ceramic capacitors placed as close as possible to device supply pins with a low impedance connection to ground plane.

Decoupling with a series inductor followed by a decoupling ceramic capacitor is more attractive when supply current requirements are not compatible with the series resistance, but the risk of LC tank resonance must be carefully considered. One more negative item against the LC tank is the higher cost.

The suggestion for the board designer is to leave space for series components and all the supply to be filled with zero ohm resistance on the prototypes. In case of noise problems,difficult to be fully anticipated, it will be possible to replace the zero Ohm resistor with a small value one or eventually with an inductor.

Regarding the bypass capacitors, the suggestion is to leave space for a small ceramic one (100 nF suggested) close to each supply pin place space for a single bigger one (10uF suggested) common to the supply rail.

Depending on the board noise level it will be possible to mount only the minimum number of capacitors effective to keep IP to perform at its best.

IBST8820 requires three different voltage supply lines, here in the following a "safe" decoupling network suggestion for each supply rail:

VDDLV

This pin feeds the 1.0V supply line.

1.0 supply line should be decoupled from the 1.0V digital supply. Suggested filtering is 1 Ohm resistor followed by a 10 uF ceramic capacitor in parallel with a 100 nF capacitor placed close to device pins.

VDDHV

This pin feeds the 1.8V supply line. This line power the receiver and transmitter path.

1.8 supply line should be decoupled from the 1.8V I/O digital supply. Suggested filtering is 1 chip ferrite bead followed by a 10 uF ceramic capacitor in parallel with 100 nF capacitor placed close to device pins.

VDDHV_TX_A/B/C/D

These pins feed the 3.3V line driver transmitter.

Due to the noise injected into the 3.3 V supply lines from transmitter operation, here four different pins are used to limit crosstalk.

Four pins should be tied together to a bulky supply plane and decoupled with appropriate capacitors. If a bulky supply plane is not available, the four supply must be locally decoupled using one 100 nF ceramic capacitor close to each one of the pins.

A.4 Board power-up sequence

The IBST8820 is tolerant to any power-up supply sequence. Reset should be released only when all the supply are present within voltage level specification.

A.5 PHY output amplitude adjusting

One key element for the performance of the Ethernet PHY is the magnetics. Based on its key parameter, the gain loss may change from different models so much to prevent the system, PHY + magnetics, to satisfy the tight transmitter output amplitude requirements without adjusting the PHY output amplitude level.

The PHY output amplitude should be adjusted by the final user once the magnetics model is selected in order to provide the correct amplitude at the MDI interface (the jack).

The following table contains the register that may be tweaked to get the correct amplitude on MDI. The nominal setting is the reference one, correct for an average magnetics gain loss.

In case the PHY is used in 10/100 BASE-T modes only, just CH_A, CH_B must be tweaked.

Table A.1 CH A output amplitude control registers

Variation +/- vout	CH_A	Shadow page	Physical Register
12.44%	mr_tx_dac_bias_prog_a[2] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[2]
	mr_tx_dac_bias_prog_a[1] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[1]
	mr_tx_dac_bias_prog_a[0] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[0]
9.29%	mr_tx_dac_bias_prog_a[2] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[2]
	mr_tx_dac_bias_prog_a[1] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[1]
	mr_tx_dac_bias_prog_a[0] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[0]
6.22%	mr_tx_dac_bias_prog_a[2] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[2]
	mr_tx_dac_bias_prog_a[1] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[1]
	mr_tx_dac_bias_prog_a[0] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[0]
2.97%	mr_tx_dac_bias_prog_a[2] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[2]
	mr_tx_dac_bias_prog_a[1] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[1]
	mr_tx_dac_bias_prog_a[0] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[0]
0%	mr_tx_dac_bias_prog_a[2] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[2]
	mr_tx_dac_bias_prog_a[1] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[1]
	mr_tx_dac_bias_prog_a[0] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[0]
-3.16%	mr_tx_dac_bias_prog_a[2] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[2]
	mr_tx_dac_bias_prog_a[1] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[1]
	mr_tx_dac_bias_prog_a[0] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[0]
-6.22%	mr_tx_dac_bias_prog_a[2] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[2]
	mr_tx_dac_bias_prog_a[1] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[1]
	mr_tx_dac_bias_prog_a[0] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[0]
-9.38%	mr_tx_dac_bias_prog_a[2] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[2]
	mr_tx_dac_bias_prog_a[1] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[1]
	mr_tx_dac_bias_prog_a[0] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[0]

Table A.2 CH B output amplitude control registers

Variation +/- vout	CH_B	Shadow page	Physical Register
12.44%	mr_tx_dac_bias_prog_b[2] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[5]
	mr_tx_dac_bias_prog_b[1] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[4]
	mr_tx_dac_bias_prog_b[0] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[3]
9.29%	mr_tx_dac_bias_prog_b[2] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[5]
	mr_tx_dac_bias_prog_b[1] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[4]
	mr_tx_dac_bias_prog_b[0] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[3]
6.22%	mr_tx_dac_bias_prog_b[2] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[5]
	mr_tx_dac_bias_prog_b[1] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[4]
	mr_tx_dac_bias_prog_b[0] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[3]
2.97%	mr_tx_dac_bias_prog_b[2] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[5]
	mr_tx_dac_bias_prog_b[1] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[4]
	mr_tx_dac_bias_prog_b[0] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[3]
0%	mr_tx_dac_bias_prog_b[2] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[5]
	mr_tx_dac_bias_prog_b[1] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[4]
	mr_tx_dac_bias_prog_b[0] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[3]
-3.16%	mr_tx_dac_bias_prog_b[2] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[5]
	mr_tx_dac_bias_prog_b[1] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[4]
	mr_tx_dac_bias_prog_b[0] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[3]
-6.22%	mr_tx_dac_bias_prog_b[2] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[5]
	mr_tx_dac_bias_prog_b[1] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[4]
	mr_tx_dac_bias_prog_b[0] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[3]
-9.38%	mr_tx_dac_bias_prog_b[2] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[5]
	mr_tx_dac_bias_prog_b[1] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[4]
	mr_tx_dac_bias_prog_b[0] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[3]

Table A.3 CH C output amplitude control registers

Variation +/- vout	CH_C	Shadow page	Physical Register
12.44%	mr_tx_dac_bias_prog_c[2] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[8]
	mr_tx_dac_bias_prog_c[1]= 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[7]
	mr_tx_dac_bias_prog_c[0]= 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[6]
9.29%	mr_tx_dac_bias_prog_c[2] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[8]
	mr_tx_dac_bias_prog_c[1]= 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[7]
	mr_tx_dac_bias_prog_c[0]= 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[6]
6.22%	mr_tx_dac_bias_prog_c[2] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[8]
	mr_tx_dac_bias_prog_c[1] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[7]
	mr_tx_dac_bias_prog_c[0] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[6]
2.97%	mr_tx_dac_bias_prog_c[2] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[8]
	mr_tx_dac_bias_prog_c[1] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[7]
	mr_tx_dac_bias_prog_c[0] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[6]
0%	mr_tx_dac_bias_prog_c[2] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[8]
	mr_tx_dac_bias_prog_c[1] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[7]
	mr_tx_dac_bias_prog_c[0] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[6]
-3.16%	mr_tx_dac_bias_prog_c[2] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[8]
	mr_tx_dac_bias_prog_c[1] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[7]
	mr_tx_dac_bias_prog_c[0] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[6]
-6.22%	mr_tx_dac_bias_prog_c[2] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[8]
	mr_tx_dac_bias_prog_c[1] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[7]
	mr_tx_dac_bias_prog_c[0] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[6]
-9.38%	mr_tx_dac_bias_prog_c[2] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[8]
	mr_tx_dac_bias_prog_c[1] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[7]
	mr_tx_dac_bias_prog_c[0] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[6]

Table A.4 CH D output amplitude control registers

Variation +/- vout	CH_D	Shadow page	Physical Register
12.44%	mr_tx_dac_bias_prog_d[2] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[11]
	mr_tx_dac_bias_prog_d[1] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[10]
	mr_tx_dac_bias_prog_d[0] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[9]
9.29%	mr_tx_dac_bias_prog_d[2] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[11]
	mr_tx_dac_bias_prog_d[1] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[10]
	mr_tx_dac_bias_prog_d[0] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[9]
6.22%	mr_tx_dac_bias_prog_d[2] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[11]
	mr_tx_dac_bias_prog_d[1] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[10]
	mr_tx_dac_bias_prog_d[0] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[9]
2.97%	mr_tx_dac_bias_prog_d[2] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[11]
	mr_tx_dac_bias_prog_d[1] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[10]
	mr_tx_dac_bias_prog_d[0] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[9]
0%	mr_tx_dac_bias_prog_d[2] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[11]
	mr_tx_dac_bias_prog_d[1] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[10]
	mr_tx_dac_bias_prog_d[0] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[9]
-3.16%	mr_tx_dac_bias_prog_d[2] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[11]
	mr_tx_dac_bias_prog_d[1] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[10]
	mr_tx_dac_bias_prog_d[0] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[9]
-6.22%	mr_tx_dac_bias_prog_d[2] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[11]
	mr_tx_dac_bias_prog_d[1] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[10]
	mr_tx_dac_bias_prog_d[0] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[9]
-9.38%	mr_tx_dac_bias_prog_d[2] = 0	write 'd20 reg 0x10[13:8]	write 'd0 reg0x1F[11]
	mr_tx_dac_bias_prog_d[1] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[10]
	mr_tx_dac_bias_prog_d[0] = 1	write 'd20 reg 0x10[13:8]	write 'd1 reg0x1F[9]